

FIG. 1

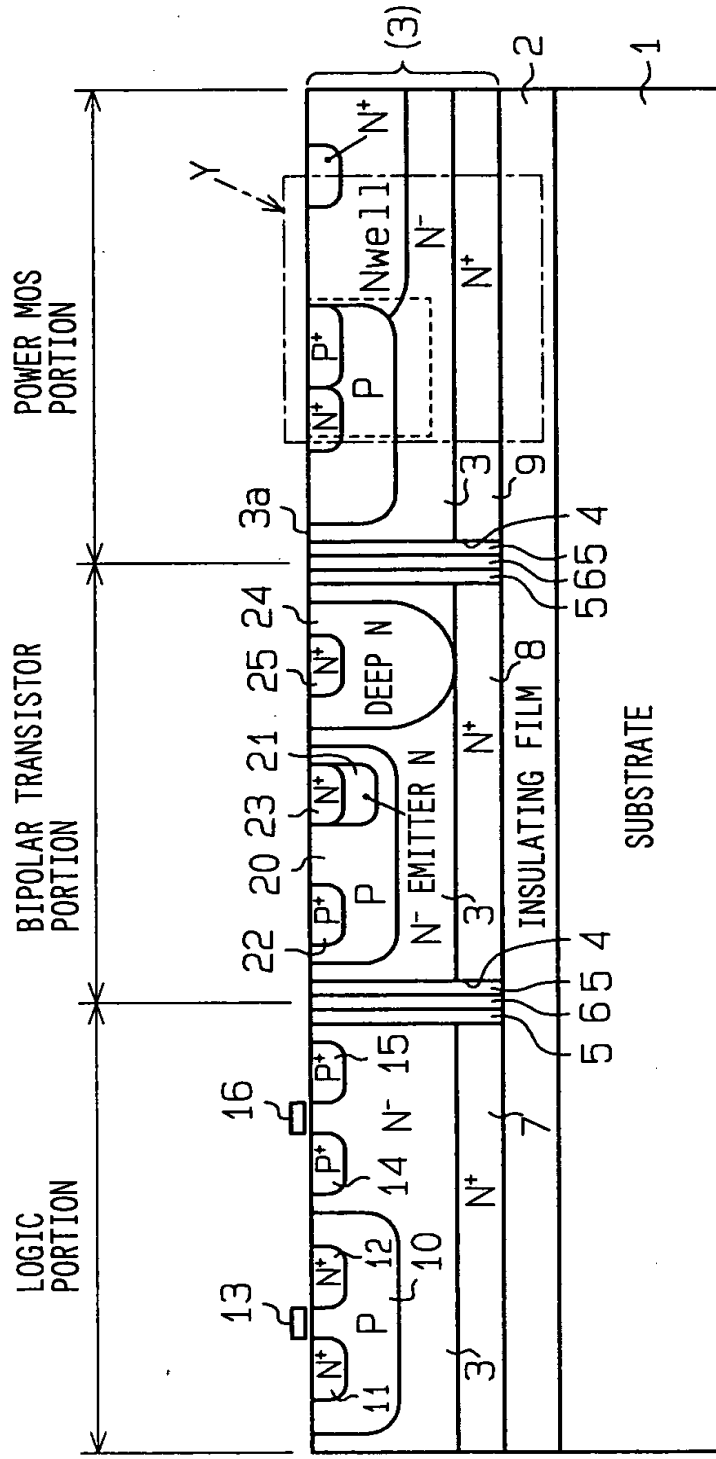


FIG. 2

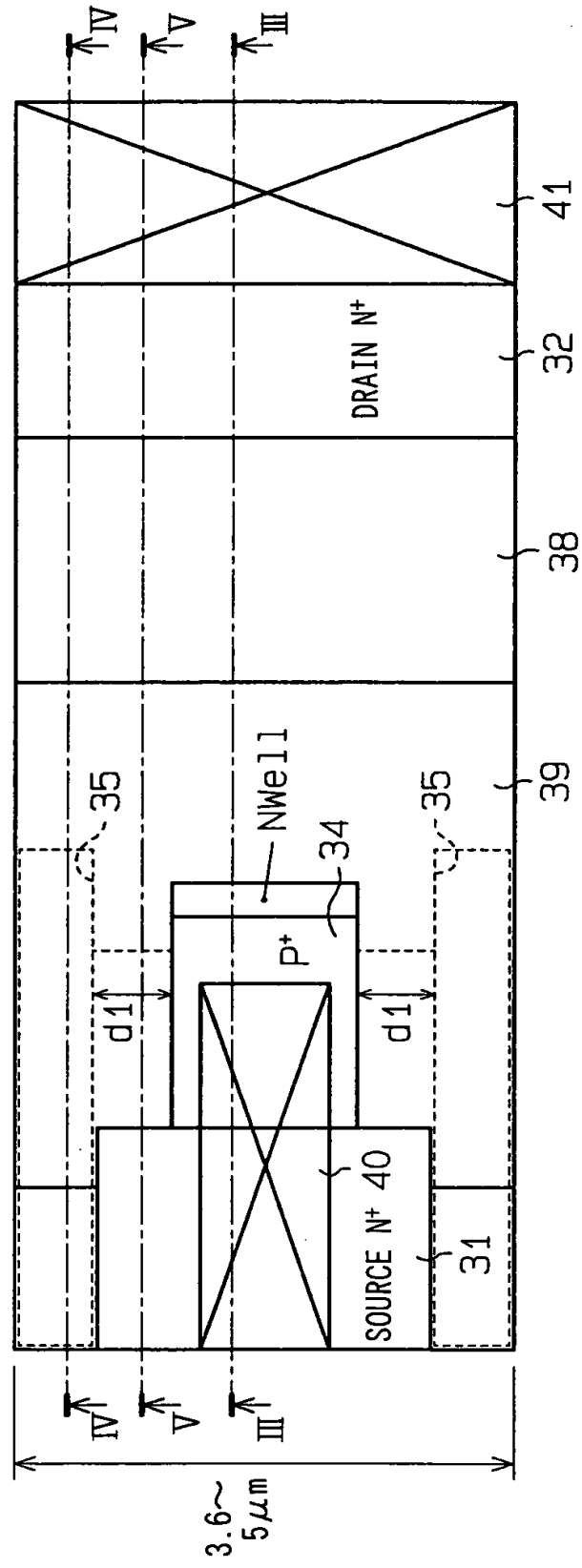
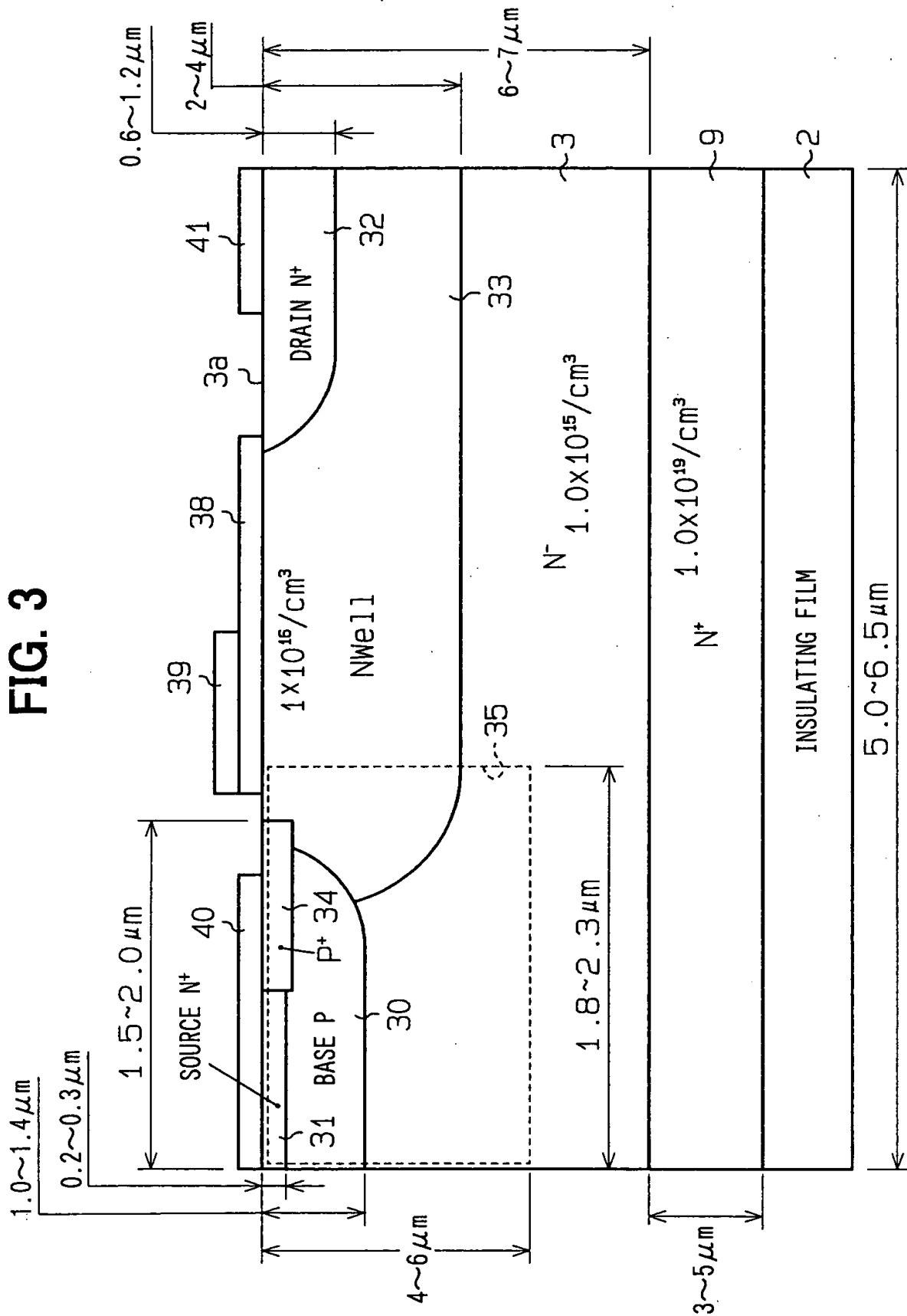
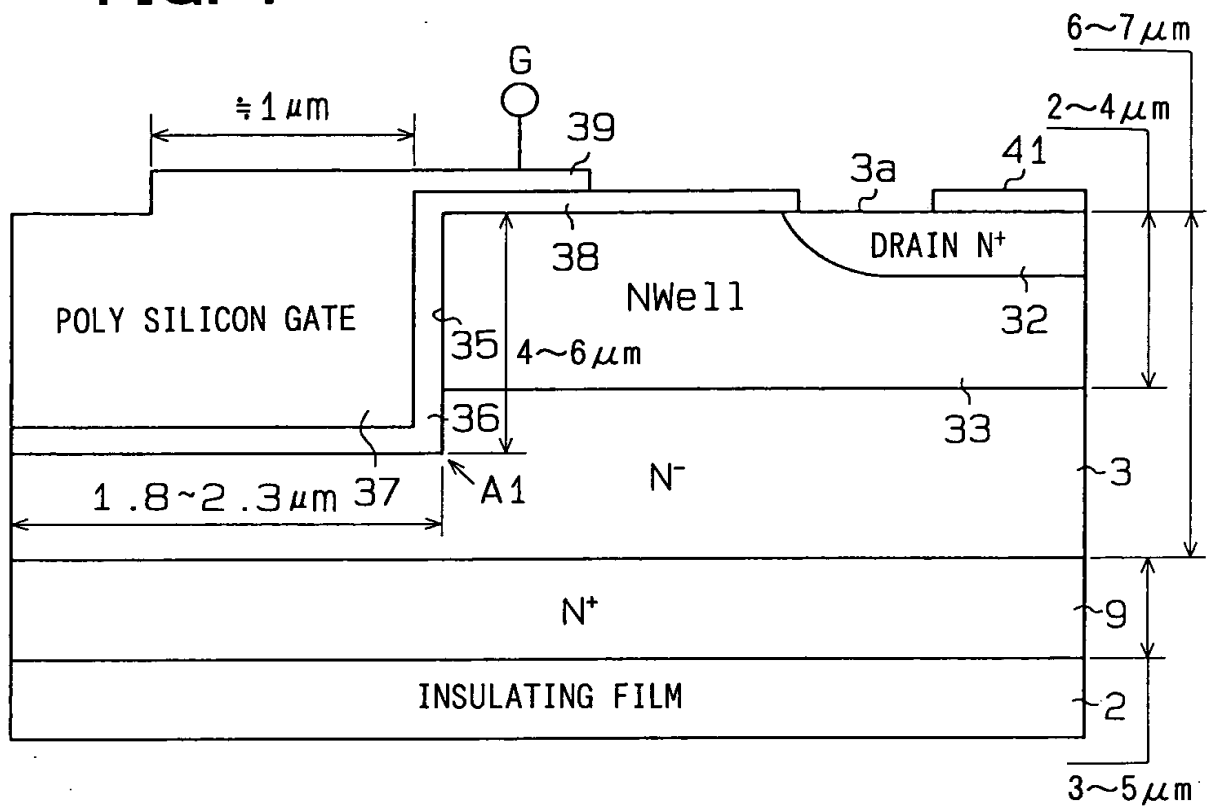


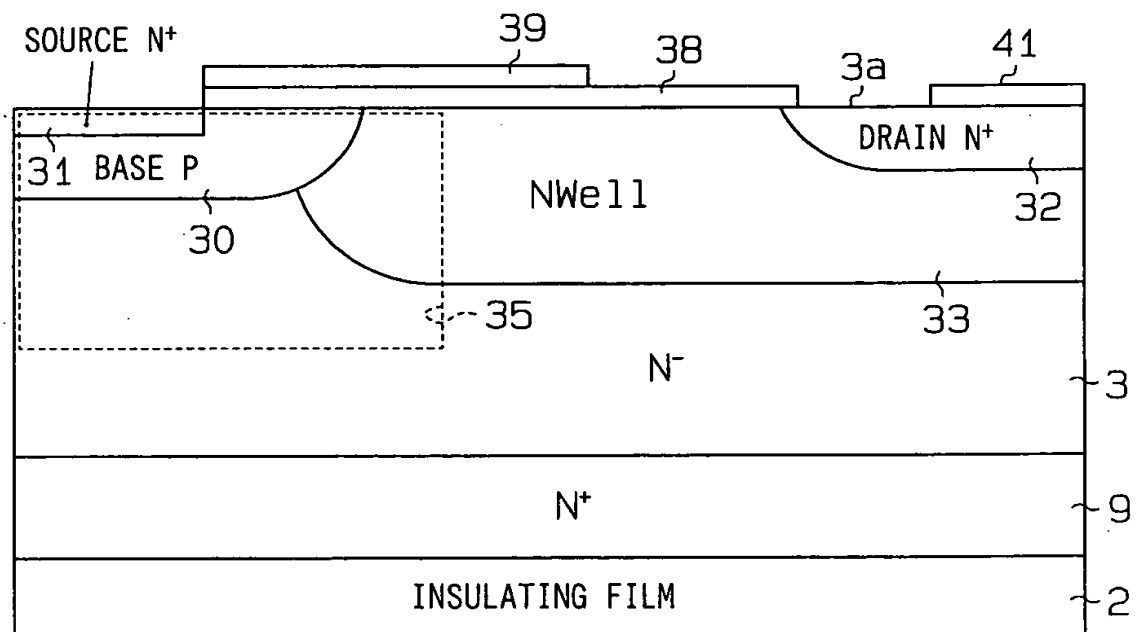
FIG. 3



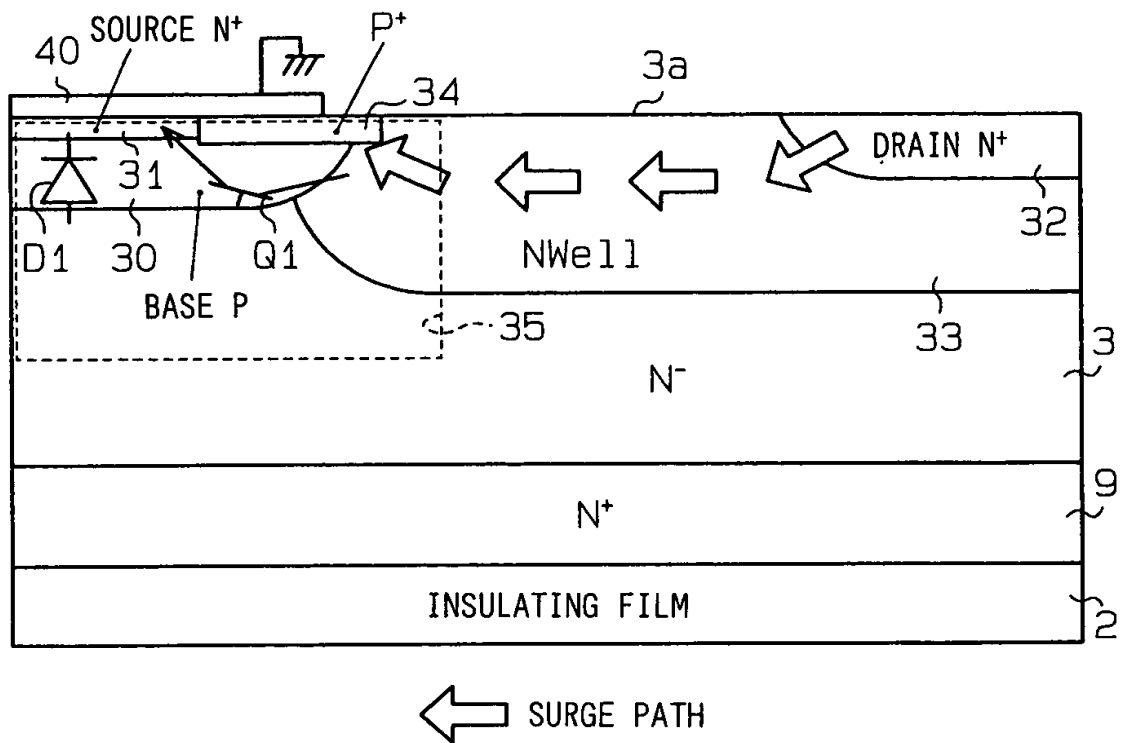
**FIG. 4**



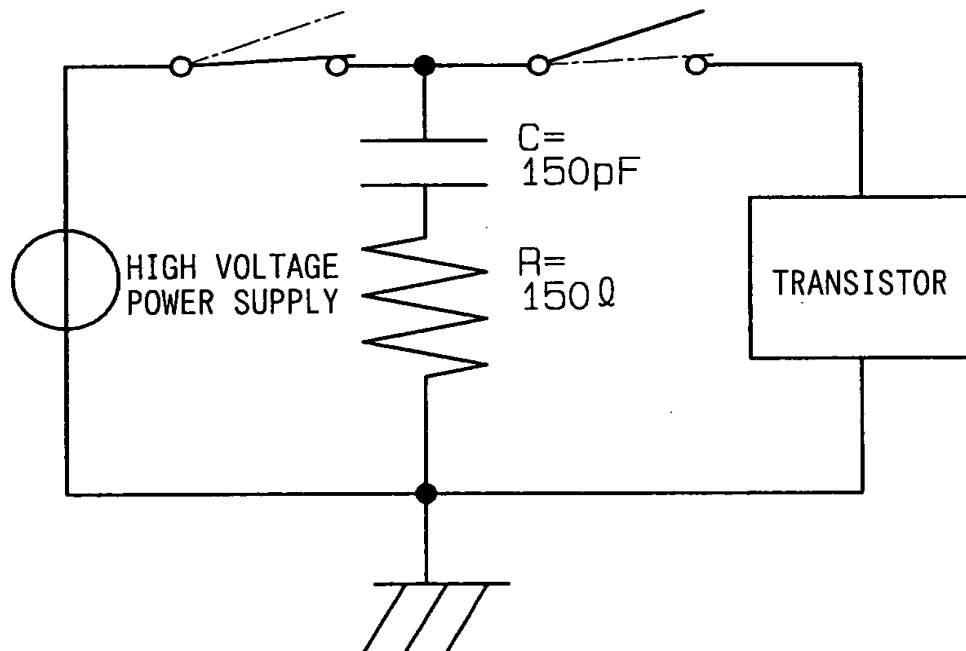
**FIG. 5**



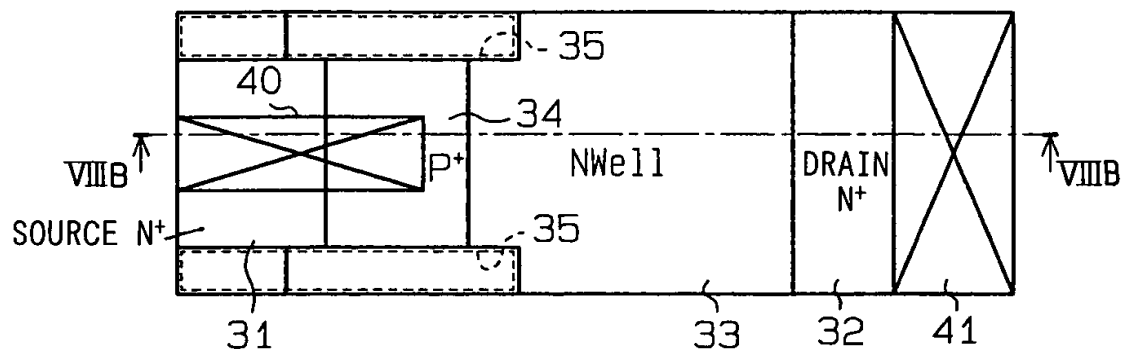
**FIG. 6**



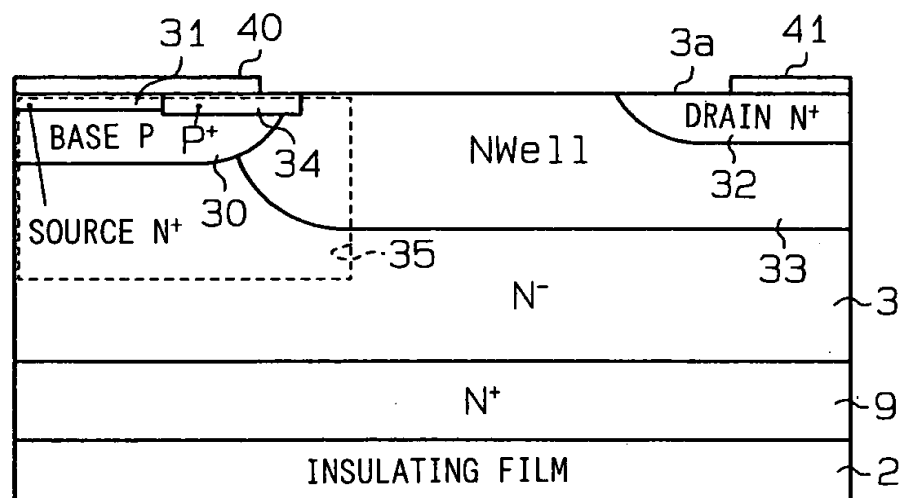
**FIG. 7**



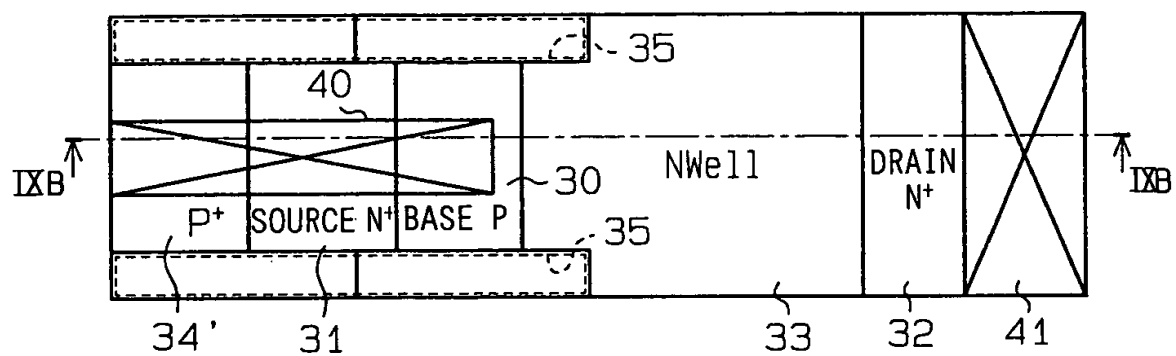
**FIG. 8A**



**FIG. 8B**



**FIG. 9A**



**FIG. 9B**

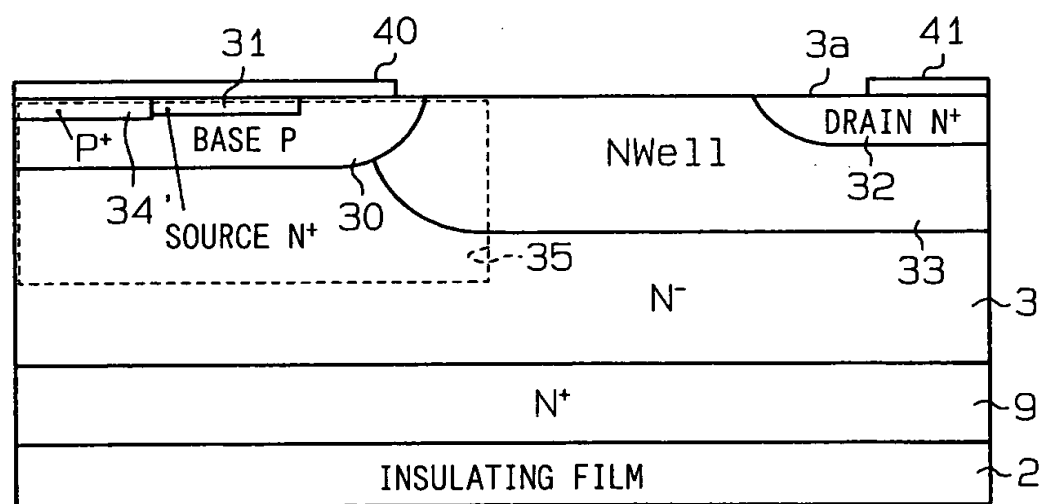
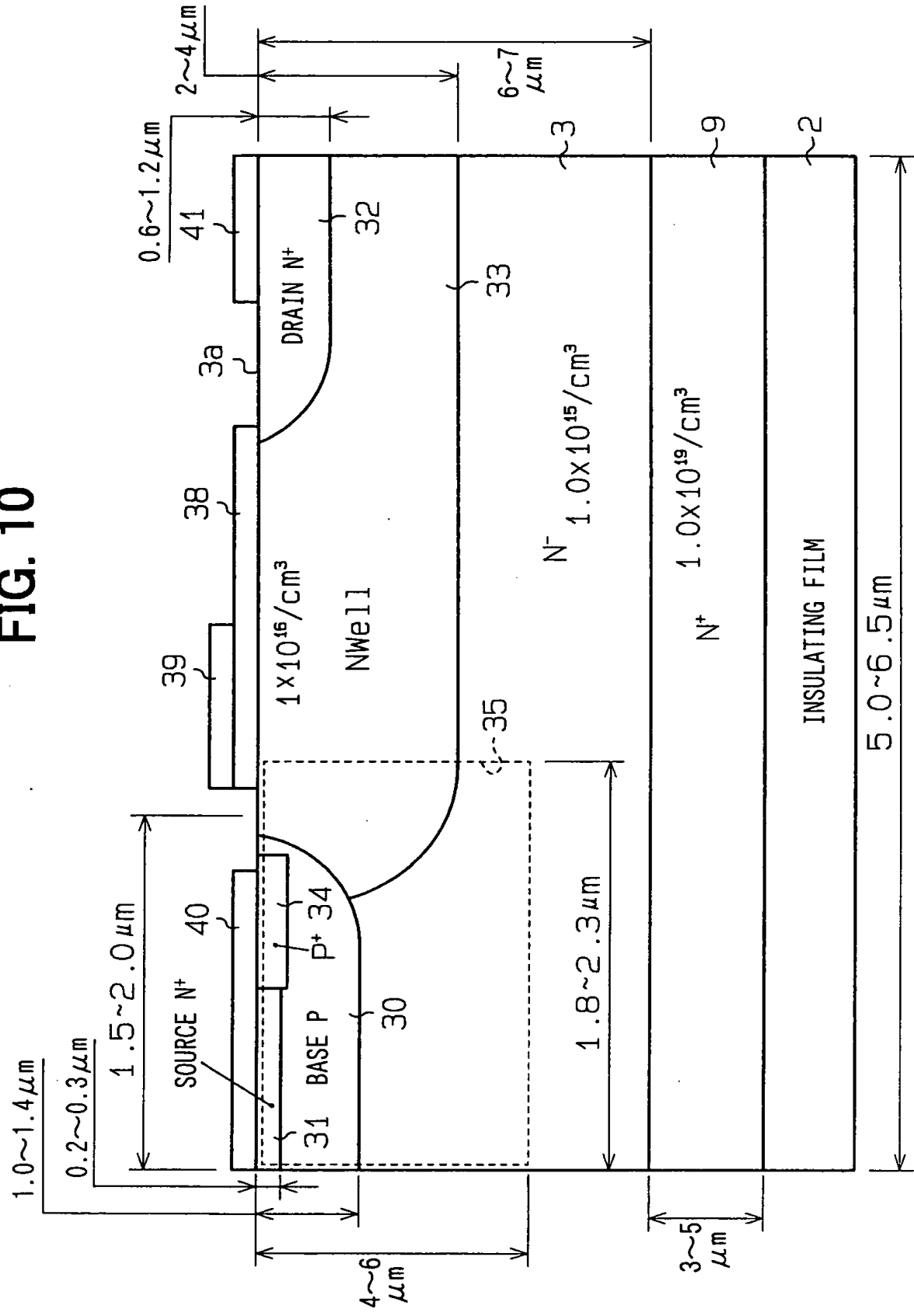
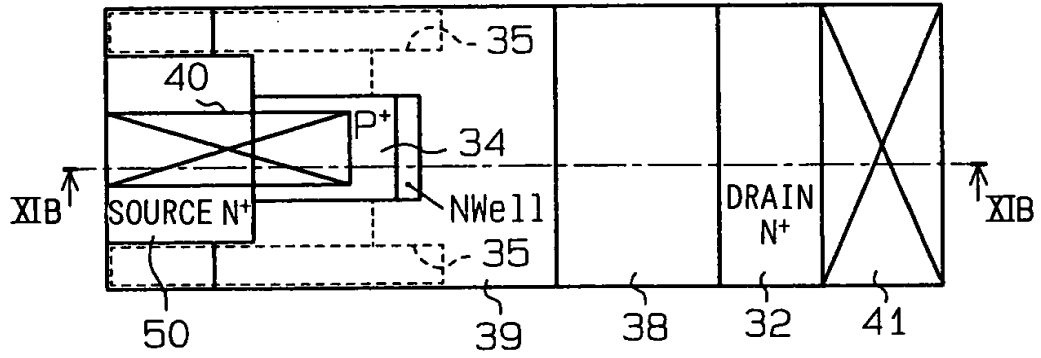


FIG. 10

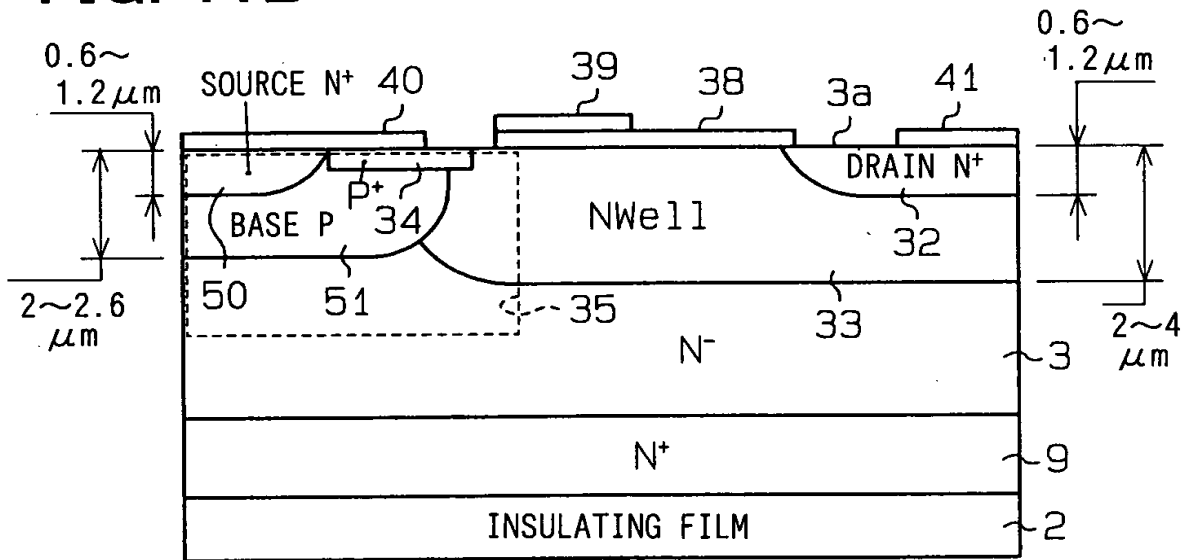




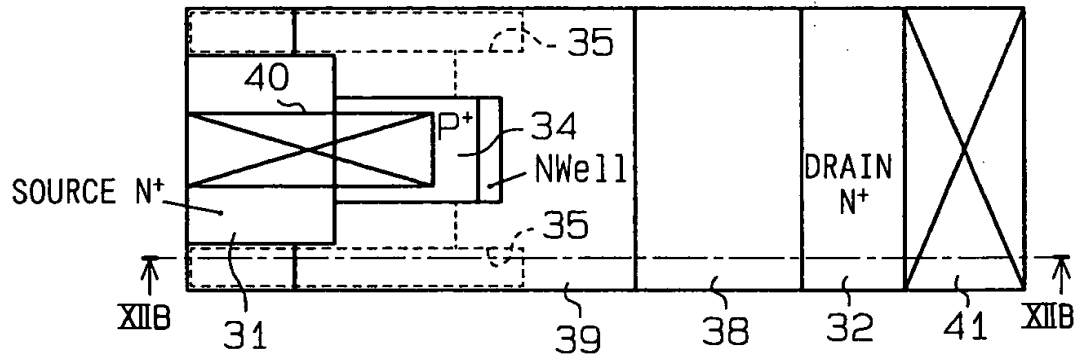
**FIG. 11A**



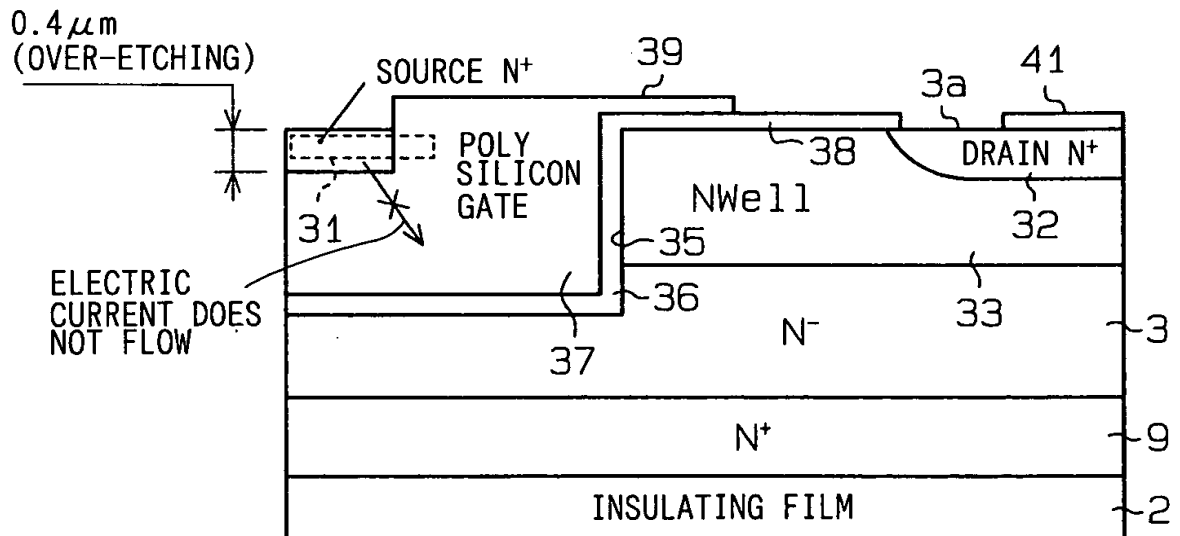
**FIG. 11B**



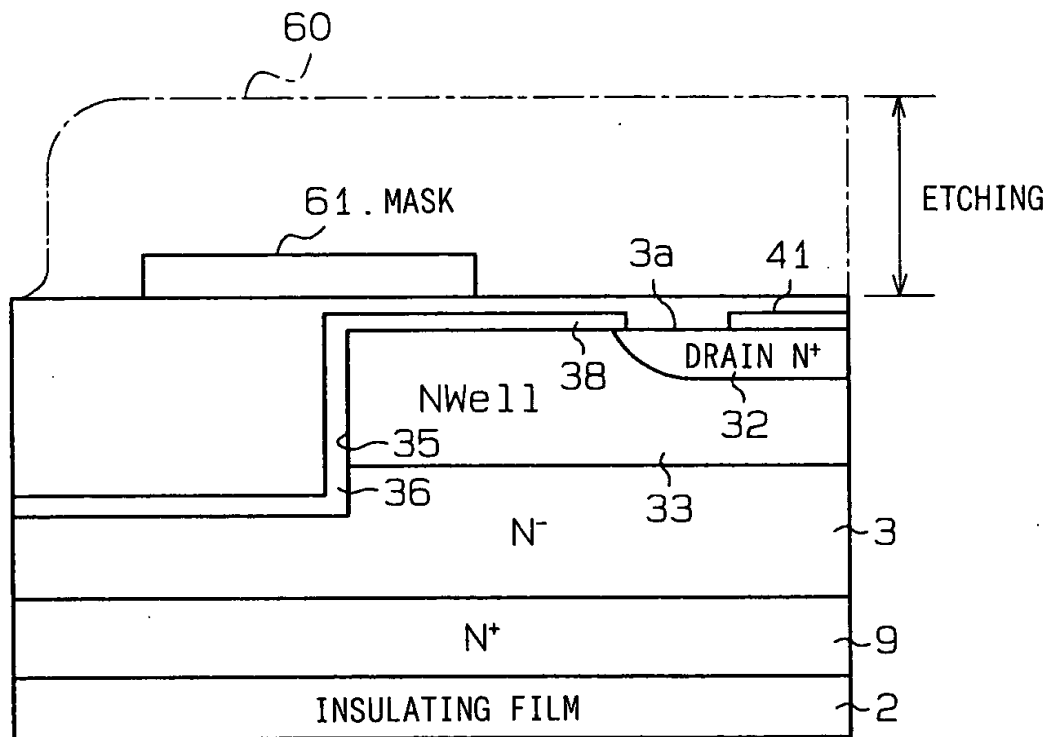
**FIG. 12A**



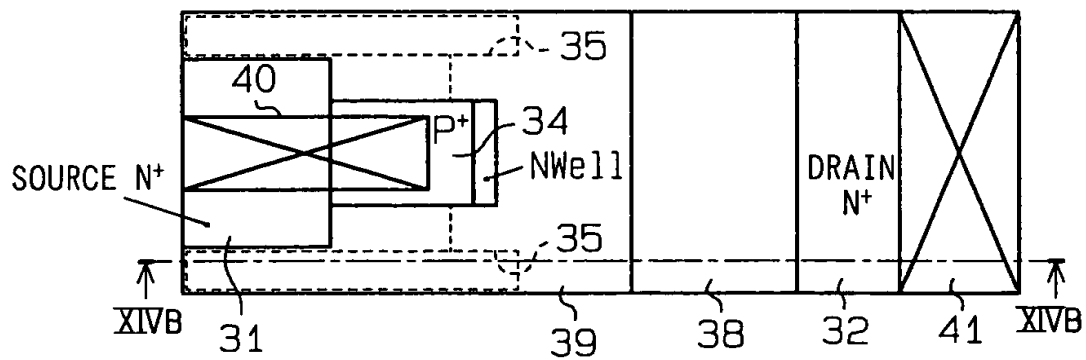
**FIG. 12B**



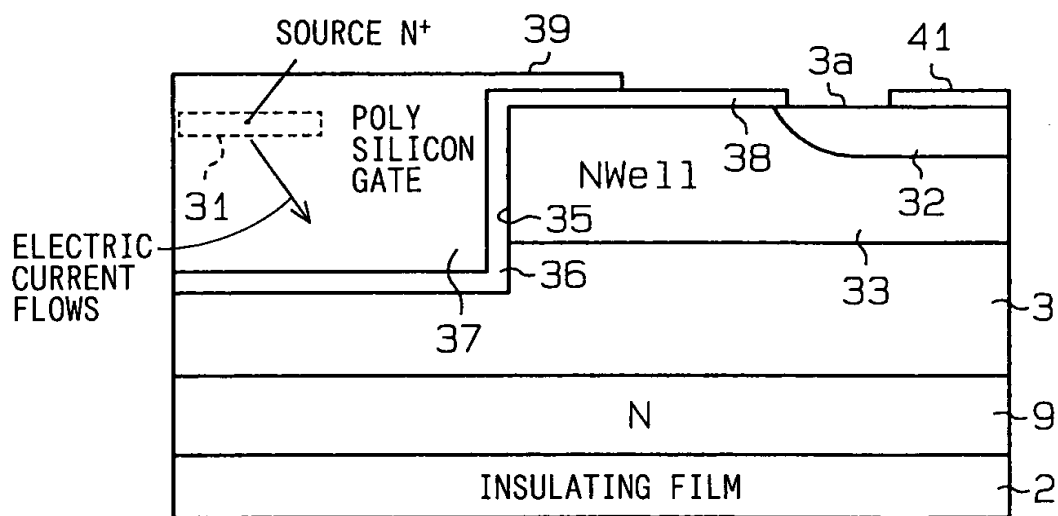
**FIG. 13**



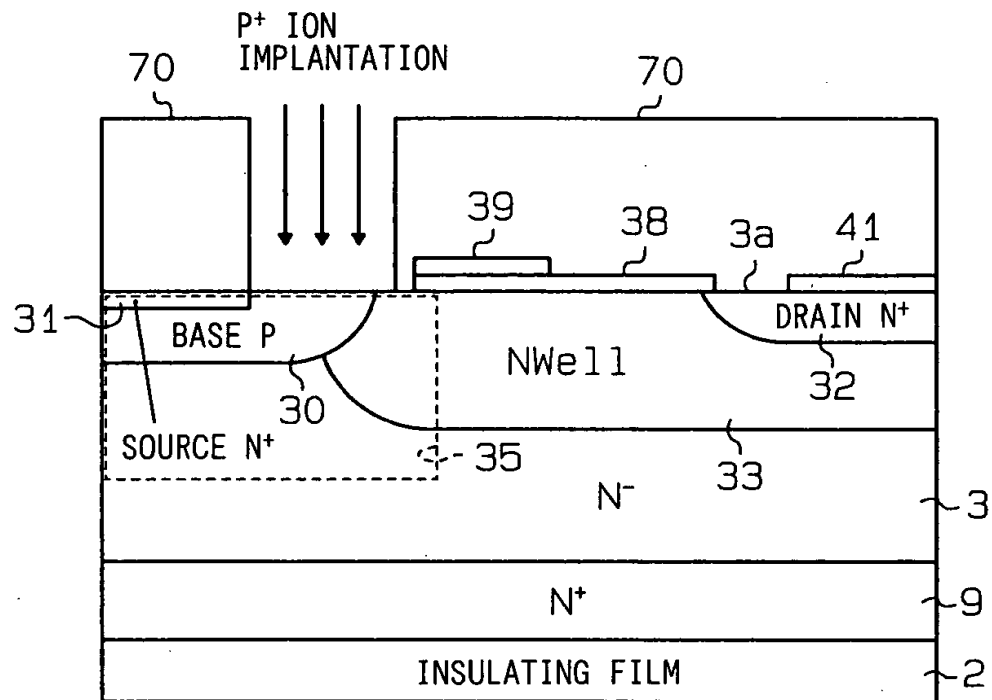
**FIG. 14A**



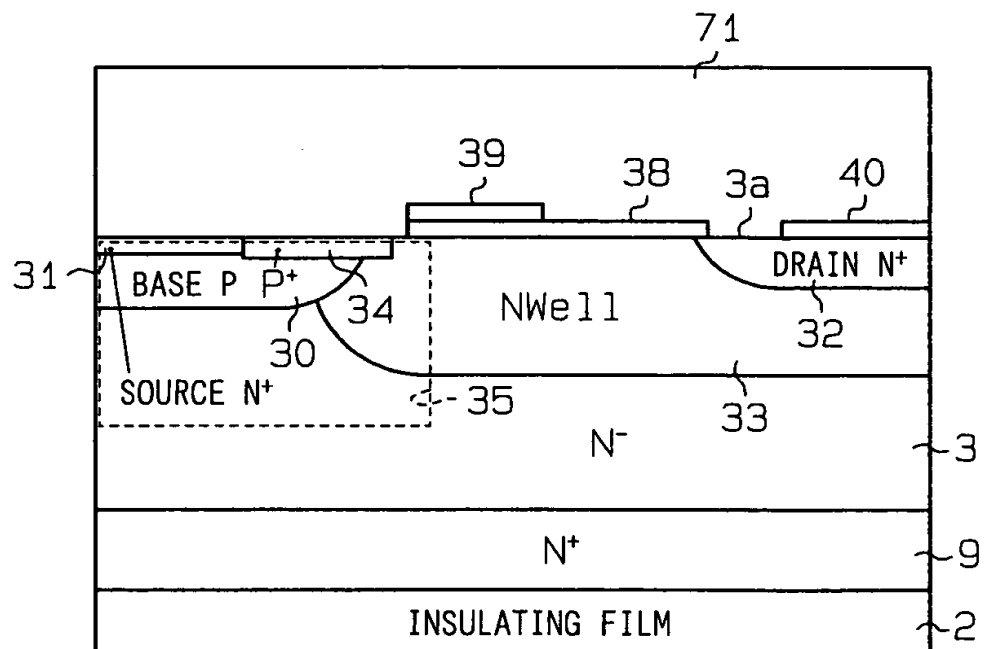
**FIG. 14B**



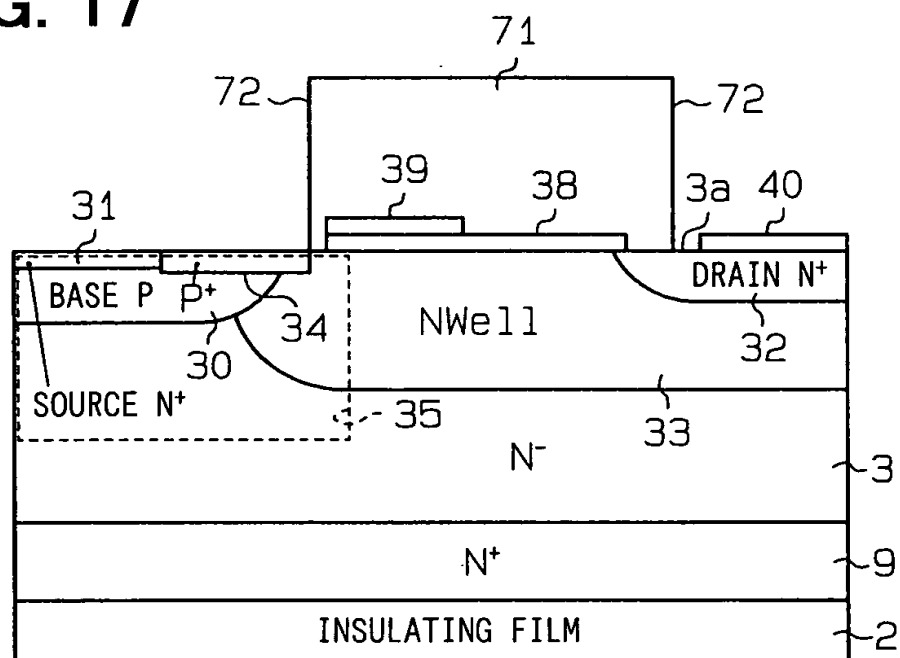
**FIG. 15**



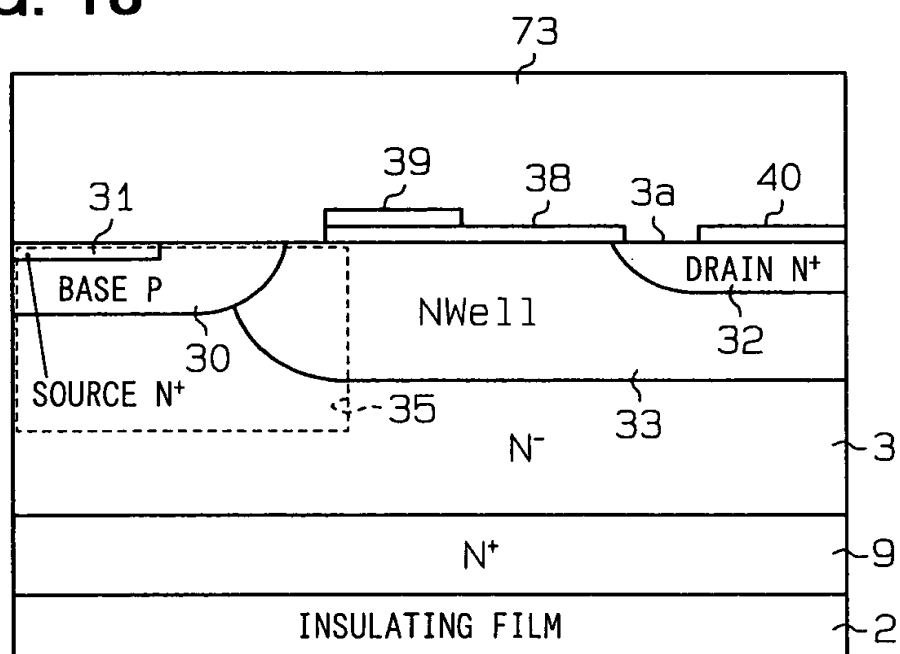
**FIG. 16**



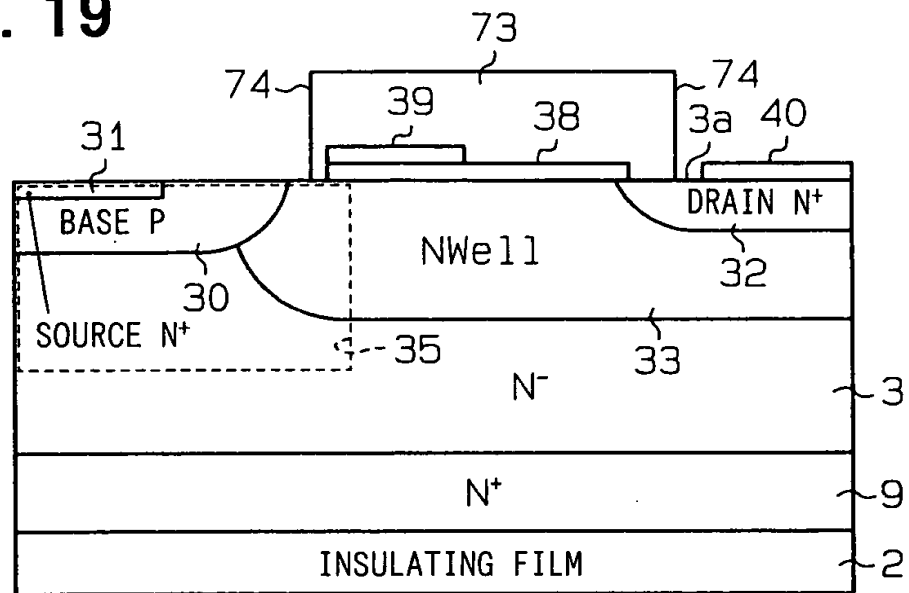
**FIG. 17**



**FIG. 18**



**FIG. 19**



**FIG. 20**

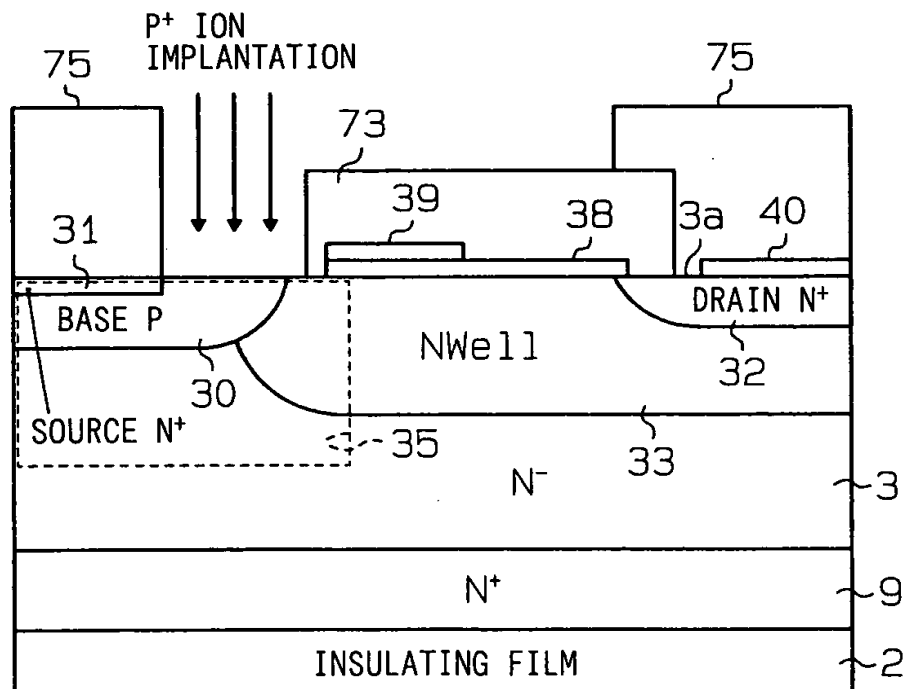


FIG. 21

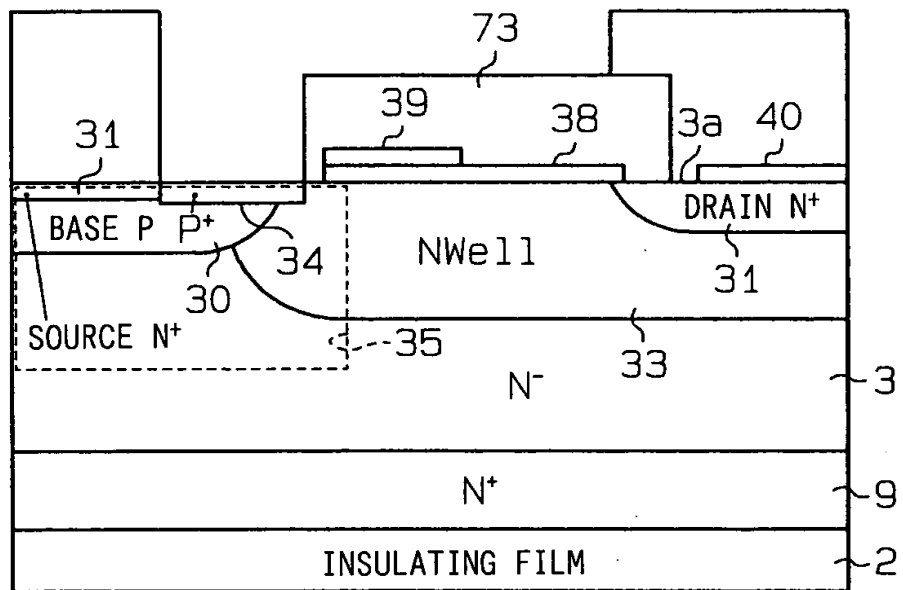
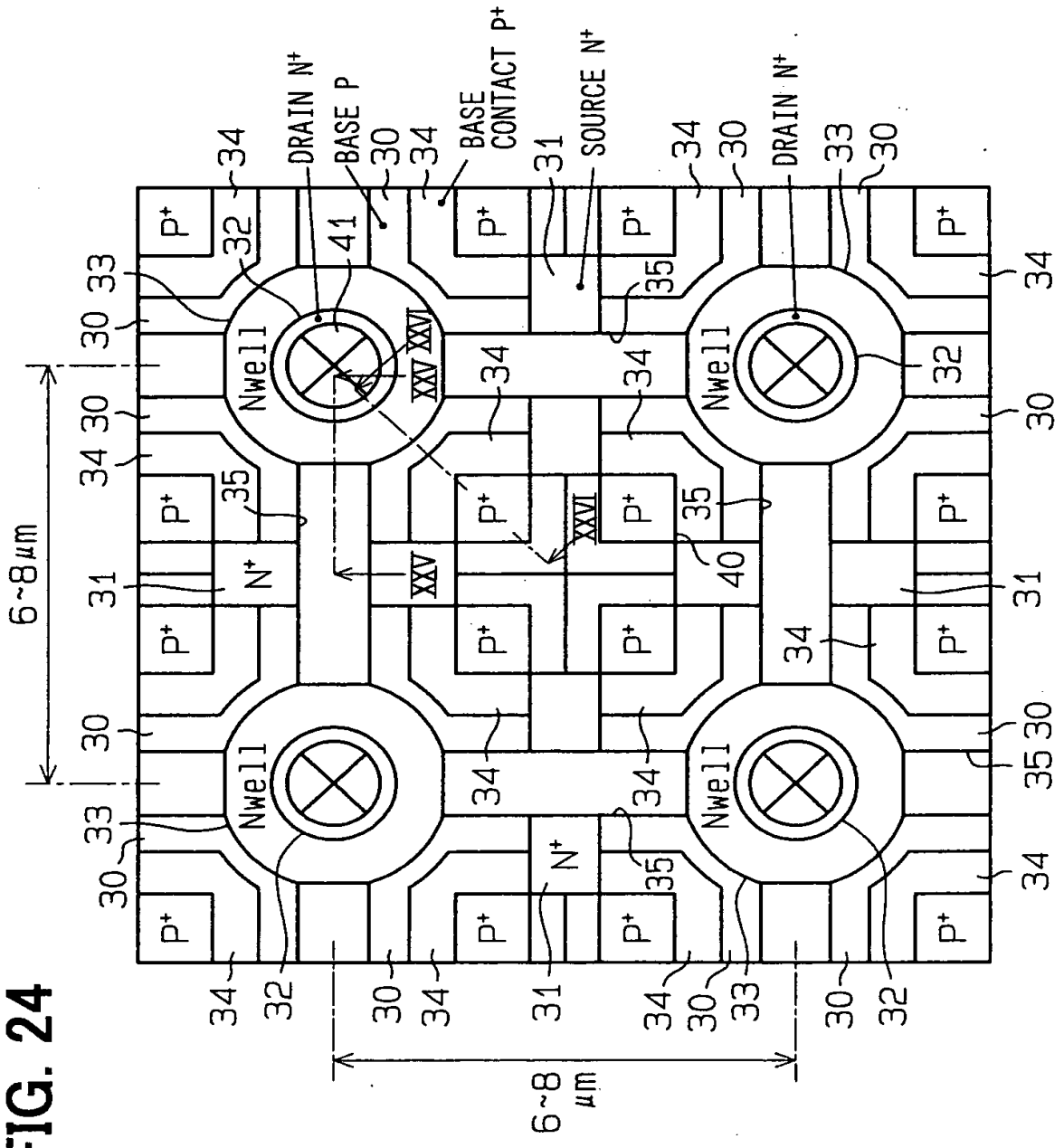




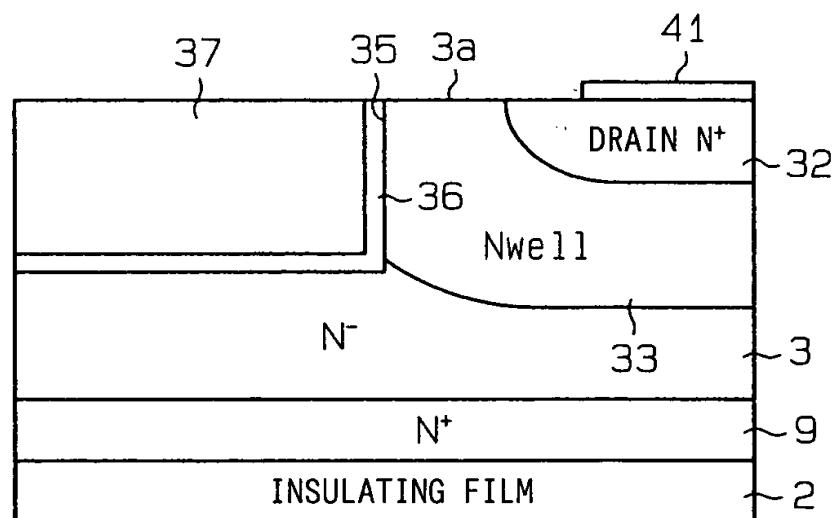
Fig. 20

Diagram illustrating a cross-sectional view of a semiconductor device. The structure includes a substrate 2, an insulating film 33, a gate stack 37, a drain region 41, and a well region 38. The gate stack 37 consists of a gate oxide 36 and a gate electrode 35. The drain region 41 contains a drain N+ layer 32. The well region 38 contains an NWell layer 35. The device is covered by an insulating film 33. Dimensions are indicated: a width of 0.6~1.2  $\mu\text{m}$  for the gate stack and a height of 2~4  $\mu\text{m}$  for the drain region.

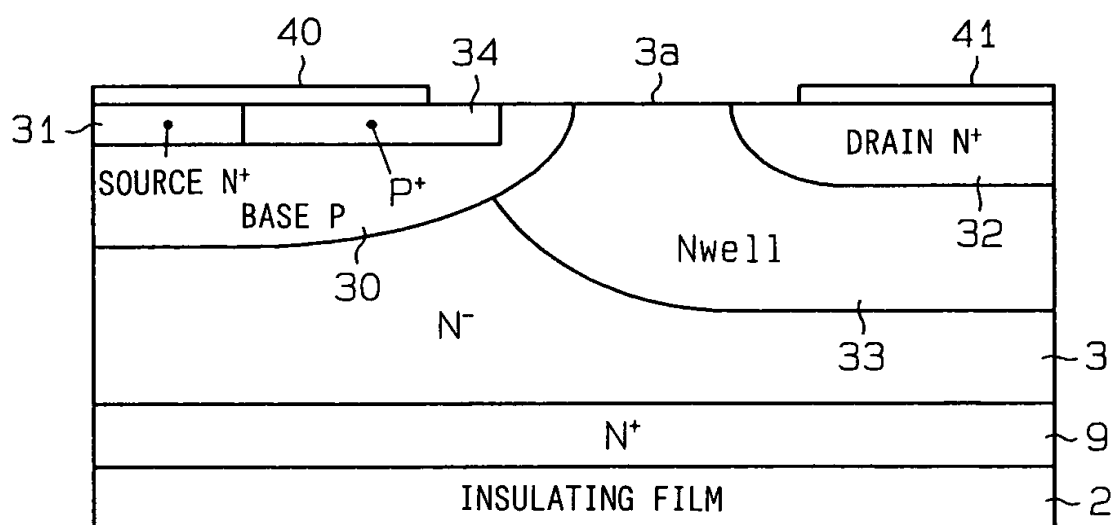
FIG. 24

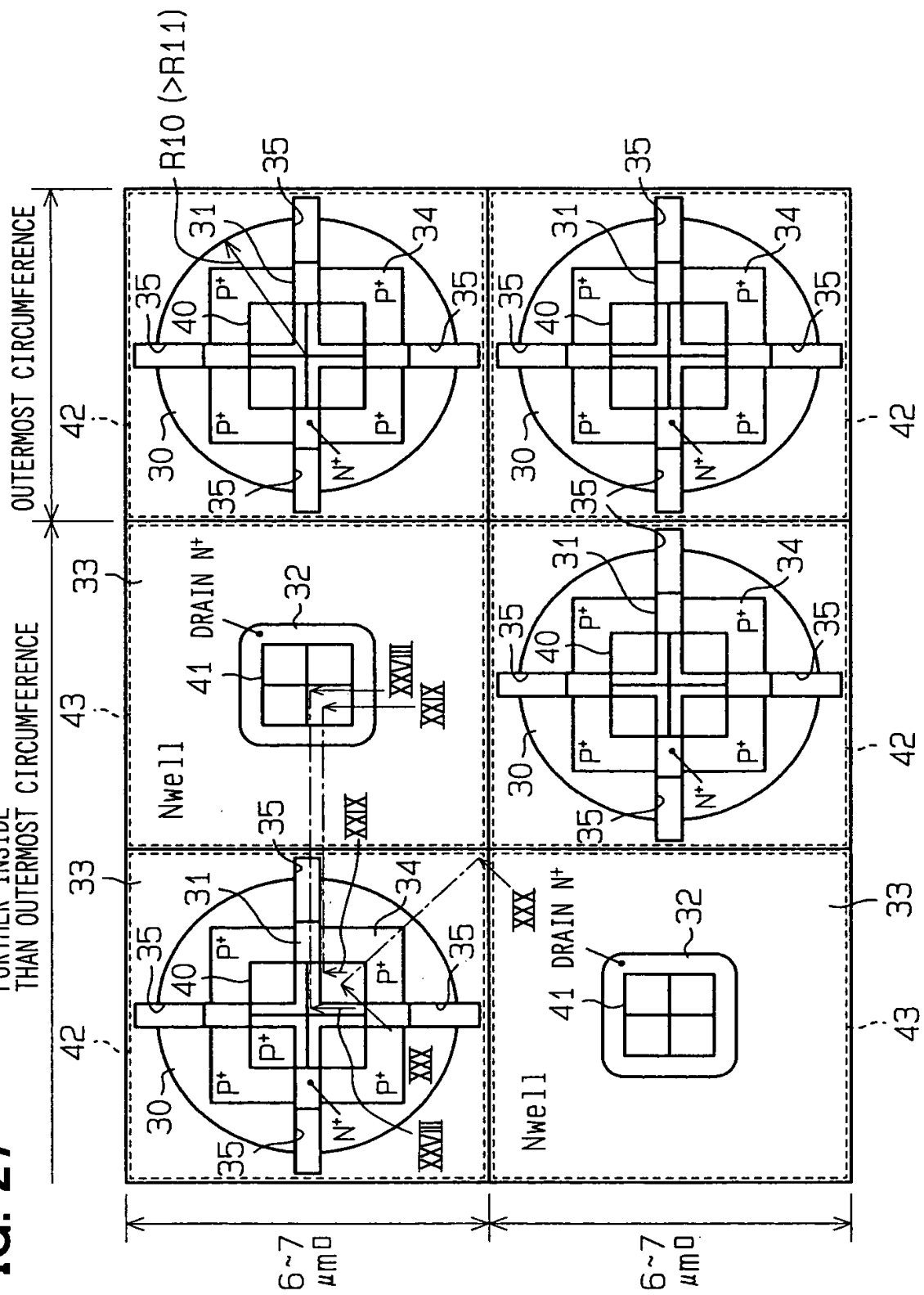


**FIG. 25**

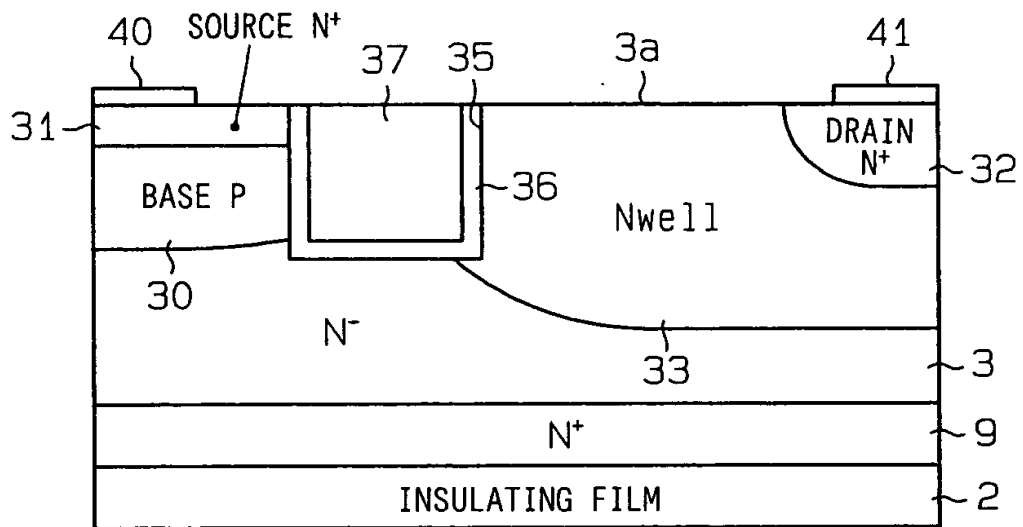


**FIG. 26**

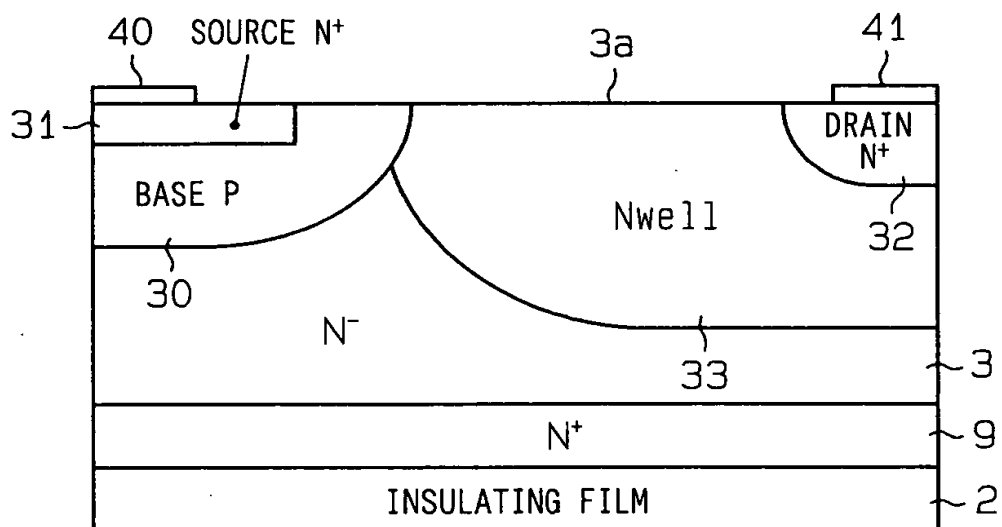


[illegible]

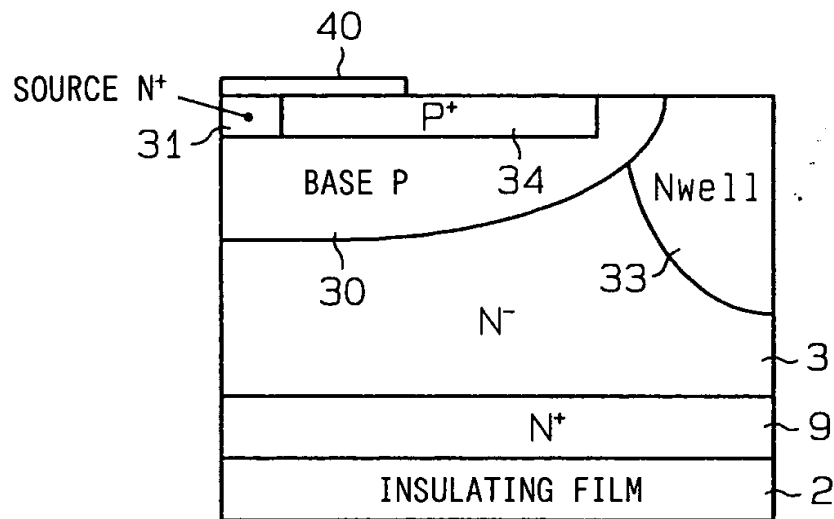
**FIG. 28**



**FIG. 29**



**FIG. 30**



**FIG. 31**  
RELATED ART

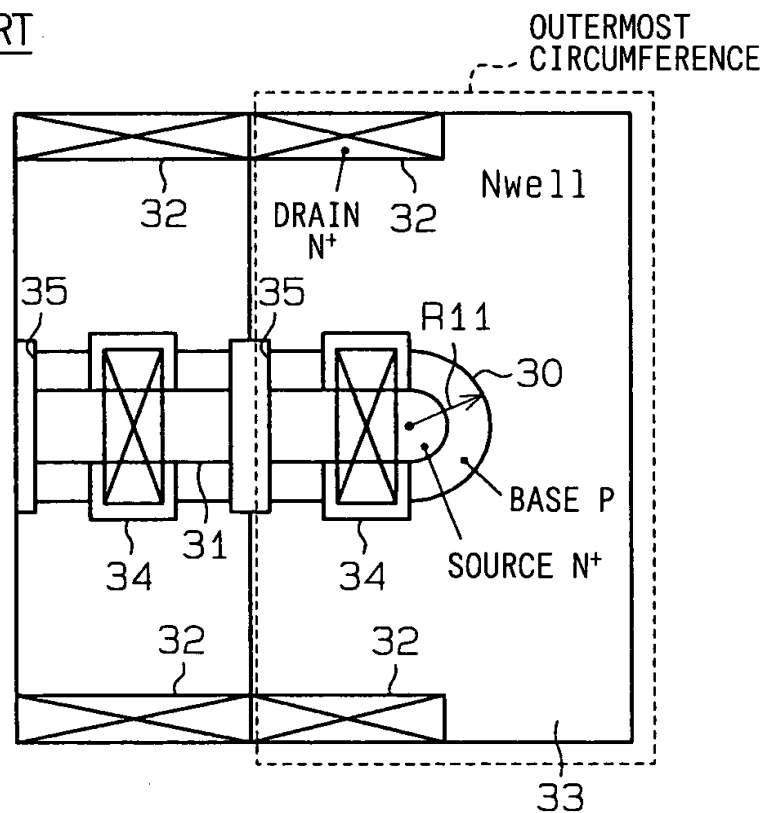


FIG. 32

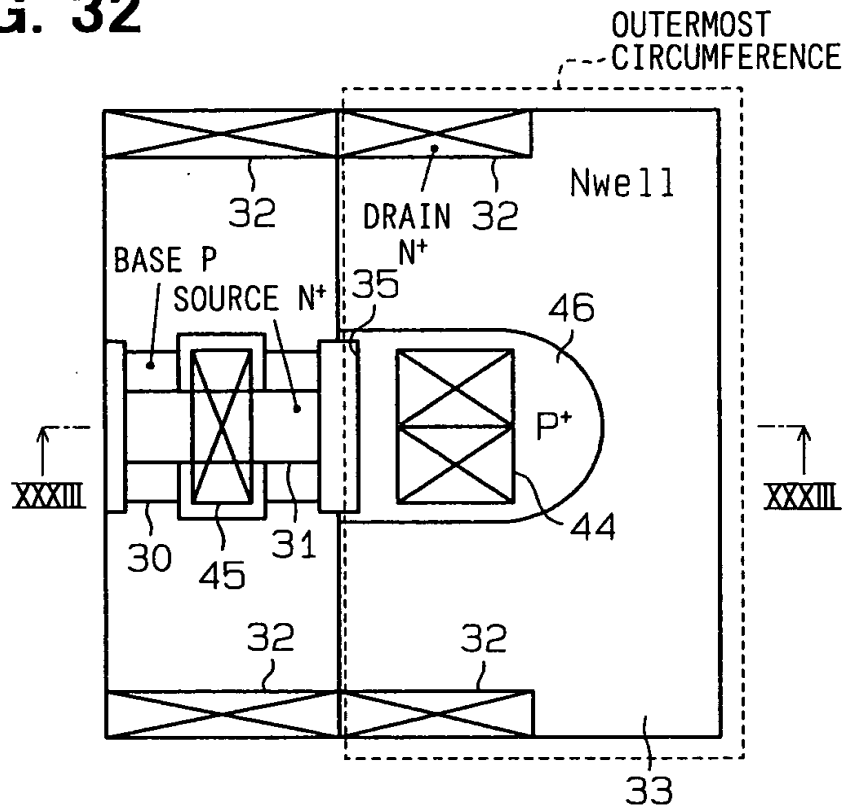
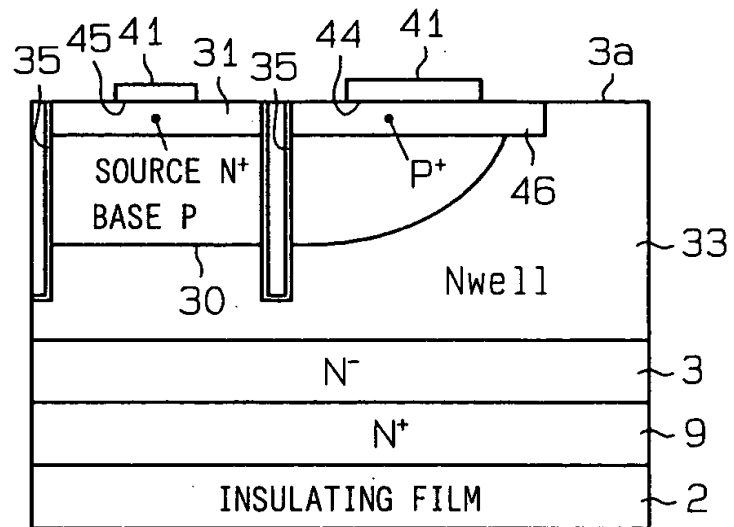
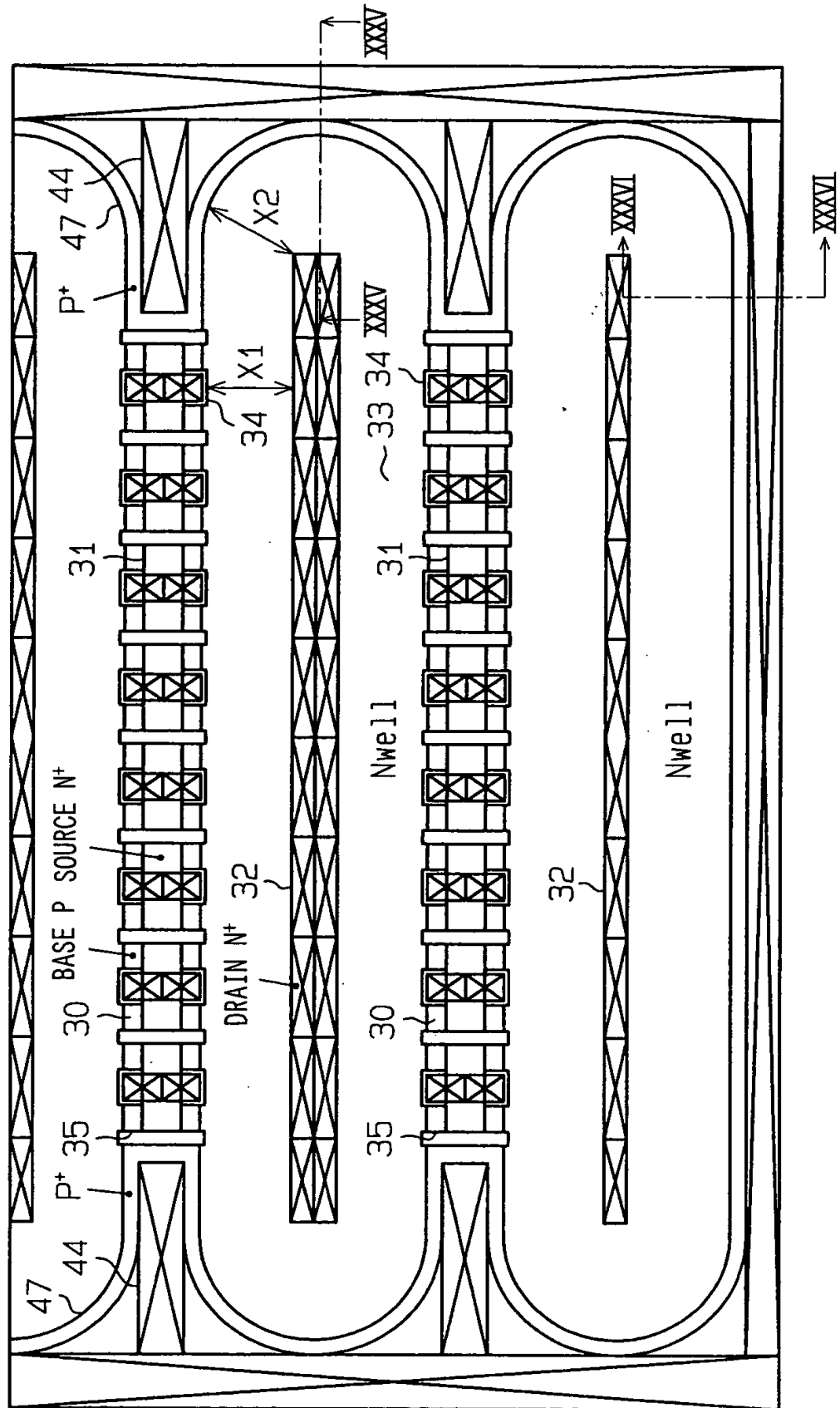


FIG. 33

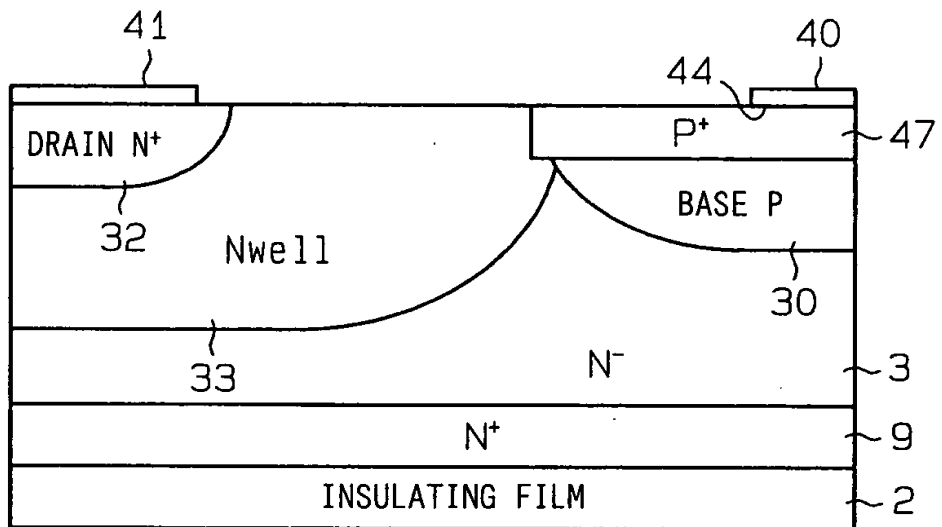


**FIG. 34**

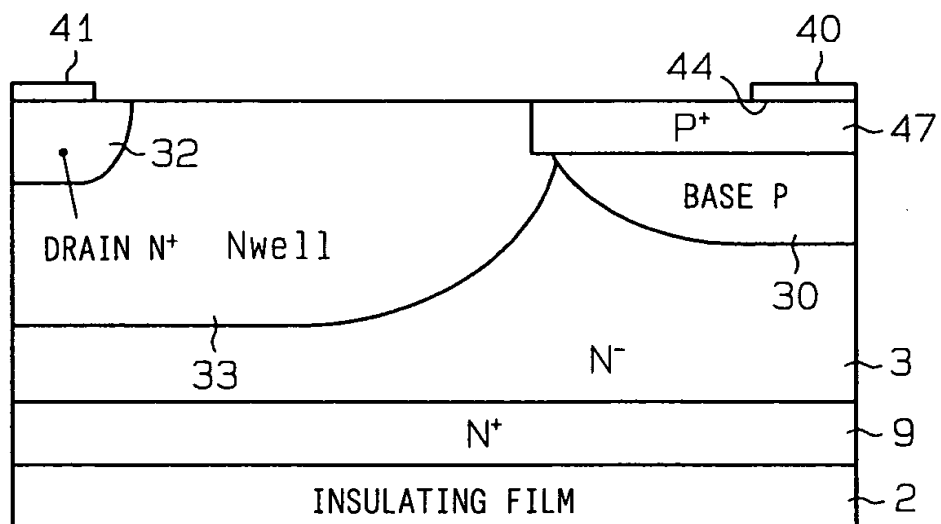




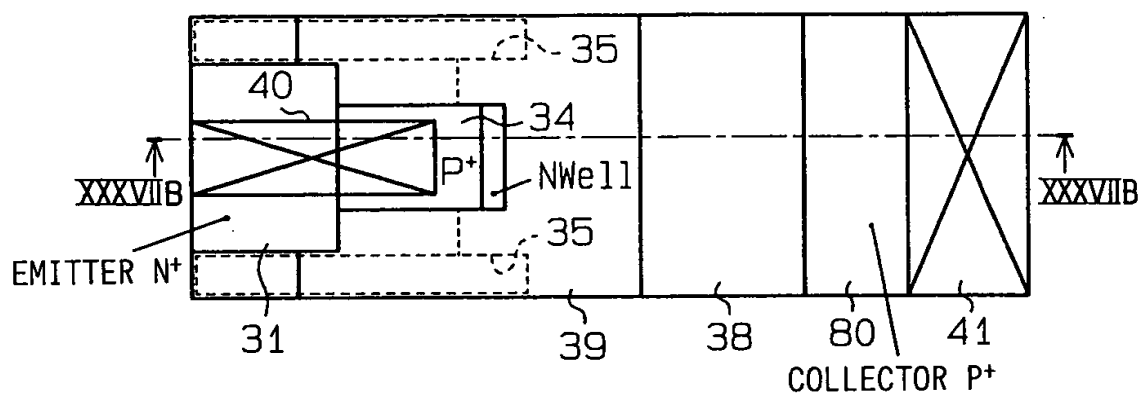
**FIG. 35**



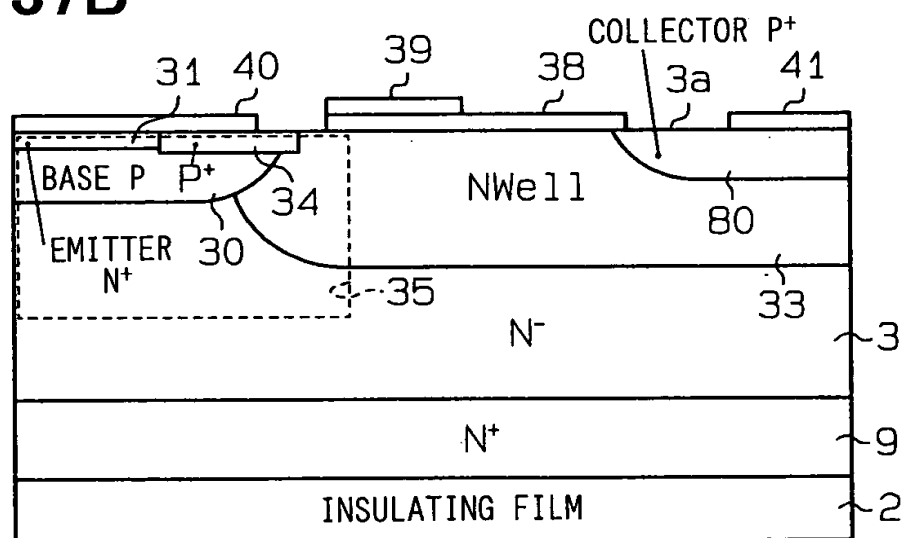
**FIG. 36**



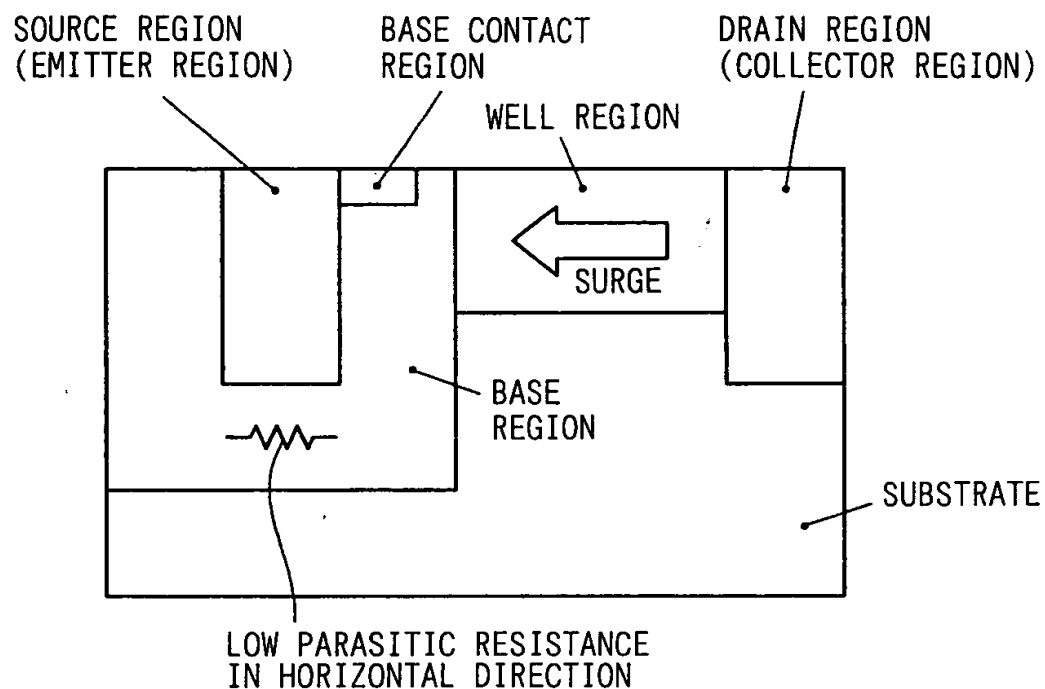
**FIG. 37A**



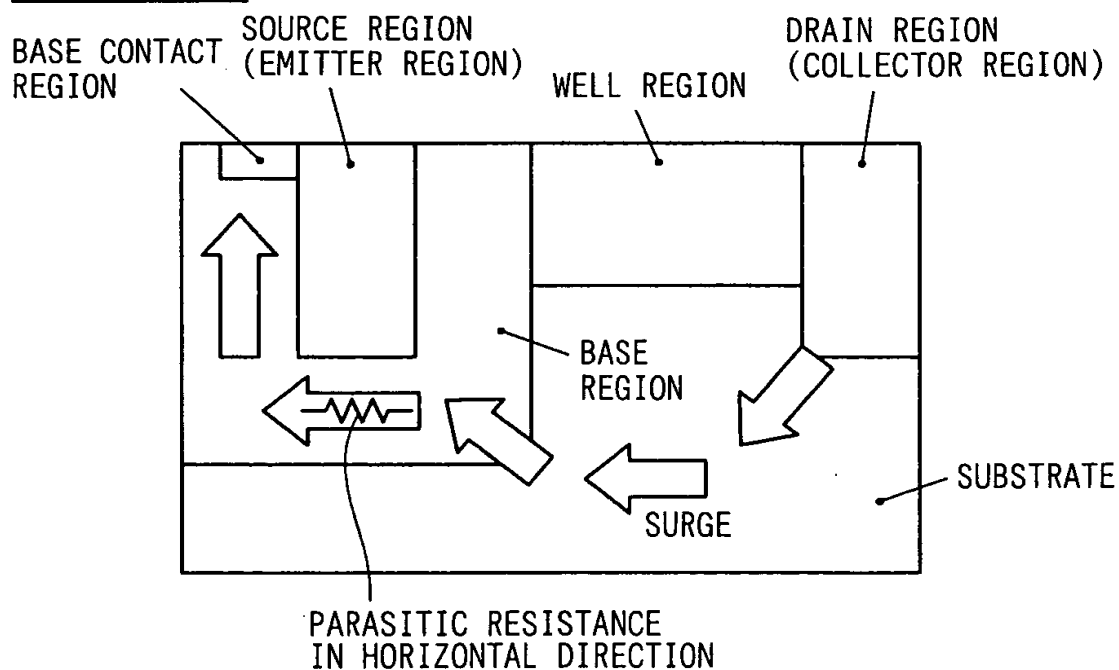
**FIG. 37B**



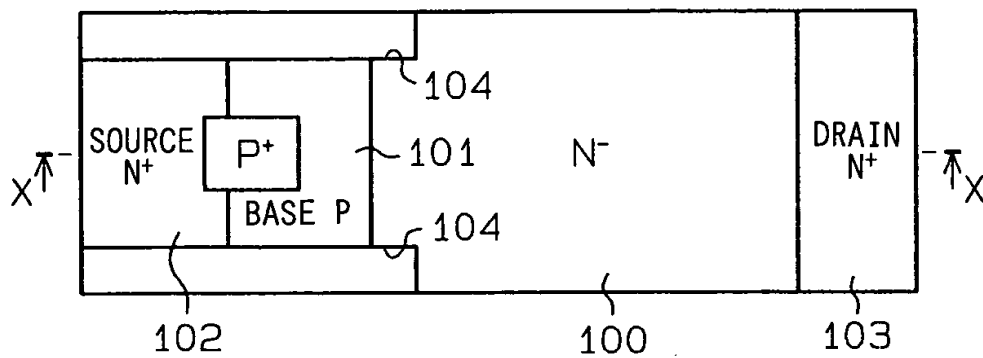
**FIG. 38**



**FIG. 39**  
RELATED ART



**FIG. 40A**  
PRIOR ART



**FIG. 40B**  
PRIOR ART

